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(54) METHOD OF MANUFACTURING SILICON SINGLE CRYSTAL

(57)Abstract:
PROBLEM TO BE SOLVED: To manufacture a silicon single crystal wafer with the CZ method under stable condition which is capable of improving in electric performance such as oxidation high withstanding voltage surely without belonging to a hole rich V region, an OSF region, and a between lattice silicon rich I region.
SOLUTION: The method of manufacturing silicon single crystal wafer and silicon single crystal are characterized in that in the silicon single crystal water grown by the Czochralski method, in N region out side of OSF ring generated in ring state at the time of heat oxidizing process for all surfaces of the wafer, no defective region is existing which is to be detected by Cu deposition.

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(54)【発明の名称】　シリコン単結晶ウエーハおよびシリコン単結晶の製造方法

(57)【要約】
【課題】　空孔リッチのＶ領域、ＯＳＦ領域、そして格子間シリコンリッチのＩ域のいずれにも属さず、かつ確実に酸化膜耐圧等の電気特性を向上させることができるＣＺ法によるシリコン単結晶ウエーハを安定した製造条件下に製造する。
【解決手段】　チョクラルスキー法により育成されたシリコン単結晶ウエーハにおいて、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域が存在しないものであることを特徴とするシリコン単結晶ウエーハ及びシリコン単結晶の製造方法。

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【特許請求の範囲】

【請求項１】　チョクラルスキー法により育成されたシリコン単結晶ウエーハにおいて、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域が存在しないものであることを特徴とするシリコン単結晶ウエーハ。

【請求項２】　チョクラルスキー法により育成されたシリコン単結晶ウエーハにおいて、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域および酸素析出が生じにくいＮｉ領域がウエーハ全面内に存在しないものであることを特徴とするシリコン単結晶ウエーハ。

【請求項３】　チョクラルスキー法によりシリコン単結晶を育成する場合において、育成されたシリコン単結晶ウエーハに熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域が存在しない無欠陥領域内で結晶を成長させることを特徴とするシリコン単結晶の製造方法。

【請求項４】　チョクラルスキー法によりシリコン単結晶を育成する場合において、引上げ中のシリコン単結晶の成長速度を漸減した場合、ＯＳＦリング消滅後に残存するＣｕデポジションにより検出される欠陥領域が消滅する境界の成長速度と、さらに成長速度を漸減した場合に格子間転移ループが発生する境界の成長速度との間の成長速度に制御して結晶を育成することを特徴とするシリコン単結晶の製造方法。

【請求項５】　チョクラルスキー法によりシリコン単結晶を育成する場合において、育成されたシリコン単結晶ウエーハに熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域および酸素析出が生じにくいＮｉ領域が存在しない領域内で結晶を成長させることを特徴とするシリコン単結晶の製造方法。

【請求項６】　チョクラルスキー法によりシリコン単結晶を育成する場合において、引上げ中のシリコン単結晶の成長速度を漸減した場合、ＯＳＦリング消滅後に残存するＣｕデポジションにより検出される欠陥領域が消滅する境界の成長速度と、さらに成長速度を漸減した場合に酸素析出が生じにくいＮｉ領域が発生する境界の成長速度との間の成長速度に制御して結晶を育成することを特徴とするシリコン単結晶の製造方法。

【請求項７】　前記結晶成長時の引上げ速度を０．５ｍｍ／ｍｉｎ以上とすることを特徴とする請求項３ないし請求項６のいずれか１項に記載したシリコン単結晶の製造方法。

【発明の詳細な説明】

【０００１】

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【発明の属する技術分野】本発明は、後述するようなＶ領域、ＯＳＦ領域およびＩ領域のいずれの欠陥領域でもなく、さらに銅デポジション処理により検出される酸化膜欠陥も形成されない、高耐圧で優れた電気特性をもつシリコン単結晶ウエーハ及びシリコン単結晶の製造方法に関するものである。

【０００２】

【従来の技術】近年は、半導体回路の高集積化に伴う素子の微細化に伴い、その基板となるチョクラルスキー法（以下、ＣＺ法と略記する）で作製されたシリコン単結晶に対する品質要求が高まってきている。特に、ＦＰＤ、ＬＳＴＤ、ＣＯＰ等のグローンイン（Ｇｒｏｗｎ－ｉｎ）欠陥と呼ばれる酸化膜耐圧特性やデバイスの特性を悪化させる、単結晶成長起因の欠陥が存在しその密度とサイズの低減が重要視されている。

【０００３】これらの欠陥を説明するに当たって、先ず、シリコン単結晶に取り込まれるベイカンシイ（Ｖａｃａｎｃｙ、以下Ｖと略記することがある）と呼ばれる空孔型の点欠陥と、インタースティシアルーシリコン（Ｉｎｔｅｒｓｔｉｔｉａｌ－Ｓｉ、以下Ｉと略記することがある）と呼ばれる格子間型シリコン点欠陥のそれぞれの取り込まれる濃度を決定する因子について、一般的に知られていることを説明する。

【０００４】シリコン単結晶において、Ｖ領域とは、Ｖａｃａｎｃｙ、つまりシリコン原子の不足から発生する凹部、穴のようなものが多い領域であり、Ｉ領域とは、シリコン原子が余分に存在することにより発生する転位や余分なシリコン原子の塊が多い領域のことであり、そしてＶ領域とＩ領域の間には、原子の不足や余分が無い（少ない）ニュートラル（Ｎｅｕｔｒａｌ、以下Ｎと略記することがある）領域が存在していることになる。そして、前記グローンイン欠陥（ＦＰＤ、ＬＳＴＤ、ＣＯＰ等）というのは、あくまでもＶやＩが過飽和な状態の時に発生するものであり、多少の原子の偏りがあっても、飽和以下であれば、欠陥としては存在しないことが判ってきた。

【０００５】この両点欠陥の濃度は、ＣＺ法における結晶の引上げ速度（成長速度）と結晶中の固液界面近傍の温度勾配Ｇとの関係から決まり、Ｖ領域とＩ領域との境界近辺にはＯＳＦ（酸化誘起積層欠陥、Ｏｘｉｄａｔｉｏｎ　Ｉｎｄｕｓｅｄ　Ｓｔａｃｋｉｎｇ　Ｆａｕｌｔ）と呼ばれる欠陥が、結晶成長軸に対する垂直方向の断面で見た時に、リング状に分布（以下、ＯＳＦリングということがある）していることが確認されている。

【０００６】これら結晶成長起因の欠陥は、通常の結晶中固液界面近傍の温度勾配Ｇが大きい炉内構造（ホットゾーン：ＨＺということがある）を使用したＣＺ引上げ機で結晶軸方向に成長速度を高速から低速に変化させた場合、図７に示したような欠陥分布図として得られる。

【０００７】そしてこれら結晶成長起因の欠陥を分類す

ると、例えば成長速度が０．６mm／ｍｉｎ前後以上と比較的高速の場合には、空孔タイプの点欠陥が集合したボイド起因とされているＦＰＤ、ＬＳＴＤ、ＣＯＰ等のグローンイン欠陥が結晶径方向全域に高密度に存在し、これら欠陥が存在する領域はＶ領域と呼ばれている（図７のライン（Ａ））。また、成長速度が０．６mm／ｍｉｎ以下の場合は、成長速度の低下に伴い、ＯＳＦリングが結晶の周辺から発生し、このリングの外側に転位ループ起因と考えられているＬ／Ｄ（Ｌａｒｇｅ　Ｄｉｓｌｏｃａｔｉｏｎ：格子間転位ループの略号、ＬＳＥＰＤ、ＬＦＰＤ等）の欠陥が低密度に存在し、これら欠陥が存在する領域はＩ領域（Ｌ／Ｄ領域ということがある）と呼ばれている。さらに、成長速度を０．４mm／ｍｉｎ前後以下と低速にすると、ＯＳＦリングがウエーハの中心に凝集して消滅し、全面がＩ領域となる（図７のライン（ｃ））。

【０００８】また、近年Ｖ領域とＩ領域の中間でＯＳＦリングの外側に、Ｎ領域と呼ばれる、空孔起因のＦＰＤ、ＬＳＴＤ、ＣＯＰも、転位ループ起因のＬＳＥＰＤ、ＬＦＰＤも存在しない領域の存在が発見されている。この領域はＯＳＦリングの外側にあり、そして、酸素析出熱処理を施し、Ｘ－ｒａｙ観察等で析出のコントラストを確認した場合に、酸素析出がほとんどなく、かつ、ＬＳＥＰＤ、ＬＦＰＤが形成されるほどリッチではないＩ領域側であると報告されている（図７のライン（Ｂ））。

【０００９】これらのＮ領域は、通常の方法では、成長速度を下げた時に成長軸方向に対して斜めに存在するため、ウエーハ面内では一部分にしか存在しなかった。このＮ領域について、ボロンコフ理論（Ｖ．Ｖ．Ｖｏｒｏｎｋｏｖ；Ｊｏｕｒｎａｌ　ｏｆ　Ｃｒｙｓｔａｌ　Ｇｒｏｗｔｈ，５９（１９８２）６２５～６４３）では、引上げ速度（Ｖ）と結晶固液界面軸方向温度勾配（Ｇ）の比であるＶ／Ｇというパラメータが点欠陥のトータルな濃度を決定すると唱えている。このことから考えると、面内で引上げ速度は一定のはずであるから、面内でＧが分布を持つために、例えば、ある引上げ速度では中心がＶ領域でＮ領域を挟んで周辺でＩ領域となるような結晶しか得られなかった。

【００１０】そこで最近、面内のＧの分布を改良して、この斜めでしか存在しなかったＮ－領域を、例えば、引上げ速度Ｆを徐々に下げながら引上げた時に、ある引上げ速度でＮ領域が横全面に広がった結晶が製造できるようになった。また、この全面Ｎ領域の結晶を長さ方向へ拡大するには、このＮ領域が横に広がった時の引上げ速度を維持して引上げればある程度達成できる。また、結晶が成長するに従ってＧが変化することを考慮し、それを補正して、あくまでもＶ／Ｇが一定になるように、引上げ速度を調節すれば、それなりに成長方向にも、全面Ｎ領域となる結晶が拡大できるようになった。

【００１１】このＮ領域をさらに分類すると、ＯＳＦリングの外側に隣接するＮｖ領域（空孔の多い領域）とＩ領域に隣接するＮｉ領域（格子間シリコンが多い領域）とがあり、Ｎｖ領域では、熱酸化処理した際に酸素析出量が多く、Ｎｉ領域では酸素析出が殆ど無いことがわかっている。

【００１２】ところが上記のように、全面Ｎ領域であり、熱酸化処理した際にＯＳＦリングを発生せず、かつ全面にＦＰＤ、Ｌ／Ｄが存在しない単結晶であるにもかかわらず酸化膜欠陥が著しく発生する場合があることがわかった。そして、これが酸化膜耐圧特性のような電気特性を劣化させる原因となっており、従来の全面がＮ領域であるというだけでは不十分であり、さらなる改善が望まれていた。

【００１３】

【発明が解決しようとする課題】そこで本発明は、このような問題点に鑑みてなされたもので、空孔リッチのＶ領域、ＯＳＦ領域、そして格子間シリコンリッチのＩ領域のいずれにも属さず、かつ確実に酸化膜耐圧等の電気特性を向上させることができるＣＺ法によるシリコン単結晶ウエーハを安定した製造条件下に得ることを目的とする。

【００１４】

【課題を解決するための手段】本発明は、前記目的を達成するために為されたもので、本発明に係るシリコン単結晶ウエーハは、チョクラルスキー法により育成されたシリコン単結晶ウエーハにおいて、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域が存在しないものであることを特徴としている（請求項１）。

【００１５】このように、本発明のシリコン単結晶ウエーハは、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、特にＣｕデポジションにより検出される欠陥領域が存在しない無欠陥ウエーハであり、デバイスを作製しても酸化膜耐圧特性等の電気特性を劣化させることのない高品質のシリコンウエーハとなる。

【００１６】そして、本発明の第２の態様であるシリコン単結晶ウエーハは、チョクラルスキー法により育成されたシリコン単結晶ウエーハにおいて、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域および酸素析出が生じにくいＮｉ領域がウエーハ全面内に存在しないものであることを特徴としている（請求項２）。

【００１７】このように、本発明のシリコン単結晶ウエーハは、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、特にＣｕデポジションにより検出される欠陥領域および酸素析出が

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生じにくいＮｉ領域がウエーハ全面内に存在しない無欠陥ウエーハであり、デバイスを作製しても酸化膜耐圧特性等の電気特性を劣化させないとともに、ゲッタリング能力も高いものである。

【００１８】次に本発明に係るシリコン単結晶の製造方法は、チョクラルスキー法によりシリコン単結晶を育成する場合において、育成されたシリコン単結晶ウエーハに熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域が存在しない無欠陥領域内で結晶を成長させることを特徴としている（請求項３）。

【００１９】そして本発明に係るシリコン単結晶の製造方法は、チョクラルスキー法によりシリコン単結晶を育成する場合において、引上げ中のシリコン単結晶の成長速度を漸減した場合、ＯＳＦリング消滅後に残存するＣｕデポジションにより検出される欠陥領域が消滅する境の成長速度と、さらに成長速度を漸減した場合に格子間転移ループが発生する境界の成長速度との間の成長速度に制御して結晶を育成することを特徴としている（請求項４）。

【００２０】これらの製造方法によれば、育成されたシリコン単結晶ウエーハに熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、特にＣｕデポジションにより検出される酸化膜耐圧等の電気特性を劣化させる欠陥領域が存在しない無欠陥シリコン単結晶ウエーハを製造することができる。

【００２１】さらに本発明に係るシリコン単結晶の製造方法の第２の態様は、チョクラルスキー法によりシリコン単結晶を育成する場合において、育成されたシリコン単結晶ウエーハに熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域および酸素析出が生じにくいｉ領域が存在しない領域内で結晶を成長させることを特徴としている（請求項５）。

【００２２】加えて、本発明に係るシリコン単結晶の製造方法は、チョクラルスキー法によりシリコン単結晶を育成する場合において、引上げ中のシリコン単結晶の成長速度を漸減した場合、ＯＳＦリング消滅後に残存するＣｕデポジションにより検出される欠陥領域が消滅する境界の成長速度と、さらに成長速度を漸減した場合に酸素析出が生じにくいＮｉ領域が発生する境界の成長速度との間の成長速度に制御して結晶を育成することを特徴としている（請求項６）。

【００２３】これらの製造方法によれば、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域および酸素析出が生じにくいＮｉ領域がウエーハ全面内に存在しない無欠陥シリコン単結晶ウエーハを製造することができる。従って、酸化膜耐圧およびゲッタリング能力ともに良好な結晶を得ることができる。

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【００２４】これらの製造方法において、結晶成長時の引上げ速度を０．５ｍｍ／ｍｉｎ以上とすることが好ましい（請求項７）。このように、結晶成長時の引上げ速度を０．５ｍｍ／ｍｉｎ以上とすれば、本発明の無欠陥領域、特に酸素析出物層が形成される領域の製造マージンが拡大し、安定供給が可能になる。

【００２５】以下、本発明につき詳細に説明するが、本発明はこれらに限定されるものではない。説明に先立ち各用語につき予め解説しておく。

1）ＦＰＤ（Ｆｌｏｗ　Ｐａｔｔｅｒｎ　Ｄｅｆｅｃｔ）とは、成長後のシリコン単結晶棒からウエーハを切り出し、表面の歪み層を弗酸と硝酸の混合液でエッチングして取り除いた後、$K_2Cr_2O_7$と弗酸と水の混合液で表面をエッチング（Ｓｅｃｃｏエッチング）することによりピットおよびさざ波模様が生じる。このさざ波模様をＦＰＤと称し、ウエーハ面内のＦＰＤ密度が高いほど酸化膜耐圧の不良が増える（特開平４－１９２３４５号公報参照）。

【００２６】2）ＳＥＰＤ（Ｓｅｃｃｏ　Ｅｔｃｈ　Ｐｉｔ　Ｄｅｆｅｃｔ）とは、ＦＰＤと同一のＳｅｃｃｏエッチングを施した時に、流れ模様（ｆｌｏｗ　ｐａｔｔｅｒｎ）を伴うものをＦＰＤと呼び、流れ模様を伴わないものをＳＥＰＤと呼ぶ。この中で１０μｍ以上の大きいＳＥＰＤ（ＬＳＥＰＤ）は転位クラスターに起因すると考えられ、デバイスに転位クラスターが存在する場合、この転位を通じて電流がリークし、Ｐ－Ｎジャンクションとしての機能を果たさなくなる。

【００２７】3）ＬＳＴＤ（Ｌａｓｅｒ　Ｓｃａｔｔｅｒｉｎｇ　Ｔｏｍｏｇｒａｐｈｙ　Ｄｅｆｅｃｔ）とは、成長後のシリコン単結晶棒からウエーハを切り出し、表面の歪み層を弗酸と硝酸の混合液でエッチングして取り除いた後、ウエーハを劈開する。この劈開面より赤外光を入射し、ウエーハ表面から出た光を検出することでウエーハ内に存在する欠陥による散乱光を検出することができる。ここで観察される散乱体については学会等ですでに報告があり、酸素析出物とみなされている（Ｊｐｎ．Ｊ．Ａｐｐｌ．Ｐｈｙｓ．　Ｖｏｌ．３２，Ｐ３６７９，１９９３参照）。また、最近の研究では、八面体のボイド（穴）であるという結果も報告されている。

【００２８】4）ＣＯＰ（Ｃｒｙｓｔａｌ　Ｏｒｉｇｉｎａｔｅｄ　Ｐａｒｔｉｃｌｅ）とは、ウエーハの中心部の酸化膜耐圧を劣化させる原因となる欠陥で、Ｓｅｃｃｏエッチではピットになる欠陥が、ＳＣ－１洗浄（$NH_4OH:H_2O_2:H_2O=1:1:10$の混合液による洗浄）では選択エッチング液として働き、ＣＯＰになる。このピットの直径は１μｍ以下で光散乱法で調べる。

【００２９】5）Ｌ／Ｄ（Ｌａｒｇｅ　Ｄｉｓｌｏｃａｔｉｏｎ：格子間転位ループの略号）には、ＬＳＥＰ

Ｄ、ＬＦＰＤ等があり、転位ループ起因と考えられている欠陥である。ＬＳＥＰＤは、上記したようにＳＥＰＤの中でも１０μｍ以上の大きいものをいう。また、ＬＦＰＤは、上記したＦＰＤの中でも先端ピットの大きさが１０μｍ以上の大きいものをいい、こちらも転位ループ起因と考えられている。

【００３０】６）Ｃｕデポジション法は、半導体ウエーハの欠陥の位置を正確に測定し、半導体ウエーハの欠陥に対する検出限度を向上させ、より微細な欠陥に対しても正確に測定し、分析できるウエーハの評価法である。

【００３１】具体的なウエーハの評価方法は、ウエーハ表面上に所定の厚さの絶縁膜を形成させ、前記ウエーハの表面近くに形成された欠陥部位上の絶縁膜を破壊して欠陥部位にＣｕ等の電解物質を析出（デポジション）するものである。つまり、Ｃｕデポジション法は、Ｃｕイオンが溶存する液体の中で、ウエーハ表面に形成した酸化膜に電位を印加すると、酸化膜が劣化している部位に電流が流れ、ＣｕイオンがＣｕとなって析出することを利用した評価法である。酸化膜が劣化し易い部分にはＣＯＰ等の欠陥が存在していることが知られている。

【００３２】Ｃｕデポジションされたウエーハの欠陥部位は、集光灯下や直接的に肉眼で分析してその分布や密度を評価することができ、さらに顕微鏡観察、透過電子顕微鏡（ＴＥＭ）または走査電子顕微鏡（ＳＥＭ）等でも確認することができる。

【００３３】

【発明の実施の形態】本発明者らは、ＣＺ法によるシリコン単結晶成長に関し、Ｖ領域とＩ領域の境界近辺について、詳細に調査したところ、Ｖ領域とＩ領域の中間でＯＳＦリングの外側に、ＦＰＤ、ＬＳＴＤ、ＣＯＰの数が著しく少なく、Ｌ／Ｄも存在しないニュートラルなＮ領域を見出した。そして、このＮ領域をさらに分類すると、ＯＳＦリングの外側に隣接するＮｖ領域（空孔の多い領域）とＩ領域に隣接するＮｉ領域（格子間シリコンが多い領域）とがあり、Ｎｖ領域では、熱酸化処理した際に酸素析出量が多く、Ｎｉ領域では酸素析出が無いことがわかってきた。

【００３４】ところが、上記Ｎ領域で結晶を育成しても、酸化膜耐圧が悪いものがあり、その原因がよく判っていなかった。そこで本発明者等は、Ｃｕデポジション法によりＮ領域についてさらに詳細に調査したところ、ＯＳＦ領域の外側のＮ領域であって、析出熱処理後酸素析出が発生し易いＮｖ領域の一部にＣｕデポジション処理で検出される欠陥が著しく発生する領域があることを発見した。そして、これが酸化膜耐圧特性のような電気特性を劣化させる原因となっていることをつきとめた。

【００３５】そこで、このＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域のない領域をウエーハ全面に広げることができれば、前記種々のグローンイン欠陥がないとともに、確実に酸化膜耐圧特性等を向上することができるウエーハが得られることになる。

【００３６】本発明者等は、以下の実験を行って成長速度と欠陥分布の関係を求め、その結果に基づいて単結晶棒を育成し、ウエーハの酸化膜耐圧特性を評価した。

（実験１）図２（ａ）の装置Ａおよび図２（ｂ）の装置Ｂに示したＭＣＺ法単結晶引上げ装置（横磁場印加）の内、装置Ａは２４インチ石英ルツボに原料多結晶シリコンを１５０ｋｇチャージし、装置Ｂは２６インチ石英ルツボに原料多結晶シリコンを１６０ｋｇチャージし、各装置にて直径８インチ（直径２００ｍｍ）、方位＜１００＞のシリコン単結晶を引上げた。単結晶を引上げる際、成長速度を０．７ｍｍ／ｍｉｎから０．３ｍｍ／ｍｉｎの範囲で結晶頭部から尾部にかけて漸減させるよう制御した。またウエーハの酸素濃度が２２～２３ｐｐｍａ（ＡＳＴＭ’７９値）となるように単結晶を作製した。

【００３７】そして図３（ａ）、（ｂ）に示したように、引上げた結晶の頭部から尾部にかけて結晶軸方向に縦割り切断し、４枚のウエーハサンプルを作製した。４枚中３枚はＷＬＴ（ウエーハライフタイム）測定（測定器：ＳＥＭＩＬＡＢ　ＷＴ－８５）およびセコエッチングによりＶ領域、ＯＳＦ領域、Ｉ領域の各領域の分布状況とＦＰＤ、ＬＥＰの分布状況、そしてＯＳＦ熱処理によるＯＳＦ発生状況を調査し、各領域境界の成長速度を確認した。さらに結晶軸方向に縦割り切断したサンプルの内１枚は、図３（ｃ）に示したように、直径６インチのウエーハ形状にくり抜き加工し、１枚は鏡面加工仕上げの上、ウエーハ表面に熱酸化膜を形成した後、Ｃｕデポジション処理を施し、酸化膜欠陥の分布状況を確認した。

【００３８】本実験におけるウエーハの評価手順および評価結果の詳細を以下に述べる。

（１）引上げた単結晶棒を結晶軸方向１０ｃｍ毎の長さにブロック切断後、縦結晶軸方向に縦割り切断し、約２ｍｍ厚さのサンプルを４枚作製した。

（２）上記サンプルのうち１枚目は、ウェーハ熱処理炉内６２０℃、２時間、窒素雰囲気下において熱処理後、８００℃、４時間（窒素雰囲気下）熱処理を施し、その後１０００℃、１６時間（ドライ酸素雰囲気下）熱処理後冷却し、ＳＥＭＩＬＡＢ－８５によりウエーハライフタイム（ＷＬＴ）のマップを作成した（図４（ａ）、（ｂ）参照）。また２枚目はミラーエッチング後セコエッチングを施し、ＦＰＤおよびＬＥＰの分布を観察した。そして３枚目はＯＳＦ熱処理後セコエッチングして酸化膜を除去し、ＯＳＦの分布状況を確認した。これらの結果からＶ領域、ＯＳＦ領域、Ｉ領域の各領域を特定し、各境界の成長速度を調査した。

【００３９】装置Ａ（図２（ａ））で引上げた単結晶の各境界の成長速度（図４（ａ）参照）は、次のようにな

った。

Ｖ領域／ＯＳＦ領域境界：　０．４８４mm／ｍｉｎ、
ＯＳＦ消滅境界：　０．４７２mm／ｍｉｎ、
Ｃｕデポジション欠陥消滅境界：　０．４６７mm／ｍｉｎ、
非析出Ｎ（Ｎｉ）領域／Ｉ領域境界：　０．４５４mm／ｍｉｎ、

【００４０】装置Ｂ（図２（ｂ））で引上げた単結晶の＊る。
各境界の成長速度（図４（ｂ）参照）は、次の通りであ＊

Ｖ領域／ＯＳＦ領域境界：　０．５９６mm／ｍｉｎ、
ＯＳＦ消滅境界：　０．５８７mm／ｍｉｎ、
Ｃｕデポジション欠陥消滅境界：　０．５６６mm／ｍｉｎ、
析出Ｎ（Ｎｖ）領域／Ｎｉ領域境界：　０．５２６mm／ｍｉｎ、
Ｎｉ領域／Ｉ領域境界　：　０．５１０mm／ｍｉｎ、

【００４１】（３）上記（１）の単結晶棒の結晶軸方向に縦割り切断したサンプルの内残り１枚を直径６インチのウェーハ形状にくり抜き加工（図３（ｃ）参照）し、鏡面加工仕上げの上、ウエーハ表面に熱酸化膜形成後Ｃデポジション処理を施し、酸化膜欠陥の分布状況を確認した。評価条件は次のとおりである。

１）酸化膜：２５ｎｍ、　２）電解強度：６ＭＶ／ｃｍ、
３）電圧印加時間：５分間。

【００４２】図５にＣｕデポジションによりＮｖ領域を評価した結果図を示す。図５（ａ）はＣｕデポジションにより発生した欠陥領域の欠陥分布を、（ｂ）はＣｕデポジションによる欠陥のないＮｖ領域の欠陥分布を示す。図６（ａ）は、Ｃｕデポジションで欠陥が発生したＮｖ領域の評価結果であり、（ｂ）は、Ｃｕデポジションにより欠陥が発生しなかったＮｖ領域の評価結果である。

【００４３】以上の結果から、ＯＳＦ外側に存在するＮ領域の内、酸素析出が生じ易いＮｖ領域中に、酸化膜欠陥の生じ易いＣｕデポジションにより検出される欠陥領が存在することが判る。この領域では、Ｎｖ領域であるにもかかわらず、酸化膜耐圧が必ずしも良くない。一方、同じＮｖ領域でも、このＣｕデポジションにより検出される欠陥領域のないＮｖ領域では酸化膜耐圧が満足できる結果となることが判る。

【００４４】（実験２）次に上記結果を踏まえて装置Ｂ（図２（ｂ））を用いてＯＳＦ外側のＮ領域であって、Ｃｕデポジション欠陥領域（Ｄｎ領域）でない領域およびさらに酸素析出が生じにくいＮｉ領域も含まない領域が狙えるように成長速度を制御し、引上げた結晶から鏡面仕上げのウエーハに加工し、酸化膜耐圧特性の評価を行った。なお、Ｃ－モード測定条件は次のとおりである。

１）酸化膜：２５ｎｍ、　２）測定電極：リン・ドープ・ポリシリコン、
３）電極面積：８mm²、　４）判定電流：１ｍＡ／ｃｍ²。

その結果、酸化膜耐圧レベルは１００％の良品率であった。

【００４５】本発明者等は、以上の実験で得られた知見を踏まえた上で鋭意検討を重ね、本発明に想到したものである。本発明の第１のシリコン単結晶の製造方法は、育成されたシリコン単結晶ウエーハに熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域が存在しない無欠陥領域内で結晶を成長させることを特徴としている。

【００４６】この方法を図１に基づいて説明すると、引上げ中のシリコン単結晶の成長速度を漸減した場合、ＯＳＦリング消滅後に残存するＣｕデポジションにより検出される欠陥領域が消滅する境界の成長速度と、さらに成長速度を漸減した場合に格子間転移ループが発生する境界の成長速度との間の成長速度に制御して結晶を育成することになる。

【００４７】以上述べた方法により育成された単結晶棒から切り出されたウエーハは、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域が全く存在しない無欠陥シリコン単結晶ウエーハとなる。

【００４８】次に、第２の製造方法は、育成されたシリコン単結晶ウエーハに熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域および酸素析出が生じにくいＮｉ領域が存在しない領域内で結晶を成長させることを特徴としている。

【００４９】この方法を図１に基づいて説明すると、引上げ中のシリコン単結晶の成長速度を漸減した場合、ＯＳＦリング消滅後に残存するＣｕデポジションにより検出される欠陥領域が消滅する境界の成長速度と、さらに成長速度を漸減した場合に酸素析出が生じにくいＮｉ領域が発生する境界の成長速度との間の成長速度に制御して結晶を育成することになる。

【００５０】この製造方法により育成された単結晶棒から作製されたウエーハは、ウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であ

って、Ｃｕデポジションにより検出される欠陥領域および酸素析出が生じにくいＮｉ領域がウエーハ全面内に存在しない無欠陥シリコン単結晶ウエーハとすることができる。

【００５１】このウエーハは、酸素析出が生じにくいＮｉ領域を含まず、全てＮｖ領域であるので、無欠陥領域中に窒素およびドライ酸素雰囲気下に熱処理した際、酸素析出物層がバルク中に形成される。従って、この領域から作製したシリコン単結晶ウエーハは、酸化膜耐圧等が良好であるのみならず、優れたゲッタリング能力を持つ。

【００５２】さらに本発明品を作製する際、原料となるシリコン単結晶を０．５ｍｍ／ｍｉｎ以上の成長速度で引上げ可能な急冷構造のＣＺ引上げ装置を使用すれば、本発明の無欠陥領域、特に酸素析出物層が形成される領域（Ｎｖ－Ｄｎ）の方がより拡大し、製造上安定性を維持することができた。

【００５３】そして結晶中心部での結晶固液界面の軸方向温度勾配Ｇｃが小さく、本発明の無欠陥領域製造の際、０．５ｍｍ／ｍｉｎの成長速度が超えられないＣＺ法引上げ装置の場合、本発明品の成長速度マージンは０．０２ｍｍ／ｍｉｎを下回るため、容易に量産できなかったが、Ｇｃが大きく、本発明の無欠陥領域製造の際、０．５ｍｍ／ｍｉｎ以上の成長速度が達成できるＣＺ法引上げ装置の場合、本発明品の成長速度マージンは０．０２ｍｍ／ｍｉｎ以上であり、最大約０．０５ｍｍ／ｍｉｎを達成することができた。特に上記のように０．５ｍｍ／ｍｉｎ以上の成長速度で本発明品を製造した場合、窒素およびドライ酸素雰囲気中の熱処理後に酸素析出物層がバルグ中に形成される領域の成長速度マージンの方が容易に拡大できることがわかった。

【００５４】最後に本発明で使用したＣＺ法による単結晶引上げ装置の構成例を図２（ａ）（ｂ）により説明する。図２（ａ）に示すように、この単結晶引上げ装置３０は、引上げ室３１と、引上げ室３１中に設けられたルツボ３２と、ルツボ３２の周囲に配置されたヒータ３４と、ルツボ３２を回転させるルツボ保持軸３３及びその回転機構（図示せず）と、シリコンの種結晶を保持するシードチャック６と、シードチャック６を引上げるワイヤ７と、ワイヤ７を回転又は巻き取る巻取機構（図示せず）を備えて構成されている。ルツボ３２は、その内側のシリコン融液（湯）２を収容する側には石英ルツボが設けられ、その外側には黒鉛ルツボが設けられている。また、ヒータ３４の外側周囲には断熱材３５が配置されている。

【００５５】また、本発明の製造方法に関わる製造条件を設定するために、環状の黒鉛筒（遮熱板）９を設けている。また、図２（ｂ）に示したものは、結晶の固液界面４の外周に環状の外側断熱材１０を設けている。この外側断熱材１０は、その下端とシリコン融液２の湯面３との間に２～２０ｃｍの間隔を設けて設置されている。さらに、冷却ガスを吹き付けたり、輻射熱を遮って単結晶を冷却する筒状の冷却装置を設けることもある。別に、最近では引上げ室３１の水平方向の外側に、図示しない磁石を設置し、シリコン融液２に水平方向あるいは垂直方向等の磁場を印加することによって、融液の対流を抑制し、単結晶の安定成長をはかる、いわゆるＭＣＺ法が用いられることも多い。

【００５６】次に、上記の単結晶引上げ装置３０による単結晶育成方法について説明する。まず、ルツボ３２内でシリコンの高純度多結晶原料を融点（約１４２０°Ｃ）以上に加熱して融解する。次に、ワイヤ７を巻き出すことにより融液２の表面略中心部に種結晶の先端を接触又は浸漬させる。その後、ルツボ保持軸３３を適宜の方向に回転させるとともに、ワイヤ７を回転させながら巻き取り種結晶を引上げることにより、単結晶育成が開始される。以後、引上げ速度と温度を適切に調節することにより略円柱形状の単結晶棒１を得ることができる。

【００５７】この場合、本発明では、本発明の目的を達成するために特に重要であるのは、図２（ａ）または図２（ｂ）に示したように、引上げ室３１の湯面上の単結晶棒１中の液状部分の外周空間において、湯面近傍の結晶の融点から１４００℃までの温度域が制御できるように環状の黒鉛筒（遮熱板）９や外側断熱材１０を設けたことである。

【００５８】すなわち、この炉内温度を制御するために、例えば図２（ｂ）に示したように、引上げ室３１内に外側断熱材１０を設け、この下端と融液表面との間隔を２～２０ｃｍに設定すればよい。こうすれば、結晶中心部分の温度勾配Ｇｃ［℃／ｃｍ］と結晶周辺部分の温度勾配Ｇｅとの差が小さくなり、例えば結晶周辺の温度勾配の方が結晶中心より低くなるように炉内温度を制御することもできる。この外側断熱材１０は黒鉛筒１２の外側にあり、黒鉛筒１２の内側にも断熱筒１１を設けている。また、黒鉛筒１２の上は金属筒１３につながり、その上には冷却筒１４があって冷却媒体を流して強制冷却している。

【００５９】以上述べたシリコン単結晶の製造方法で製造されたシリコン単結晶をスライスして得られるシリコン単結晶ウエーハは、ウエーハに熱酸化処理をした際に、リング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域が存在しない無欠陥ウエーハである。あるいはウエーハ全面が熱酸化処理をした際にリング状に発生するＯＳＦの外側のＮ領域であって、Ｃｕデポジションにより検出される欠陥領域および酸素析出が生じにくいＮｉ領域がウエーハ全面内に存在しない無欠陥ウエーハである。

【００６０】なお、本発明は、上記実施形態に限定されるものではない。上記実施形態は、例示であり、本発明の特許請求の範囲に記載された技術的思想と実質的に同

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一な構成を有し、同様な作用効果を奏するものは、いかなるものであっても本発明の技術的範囲に包含される。

【００６１】例えば、上記実施形態においては、直径８インチのシリコン単結晶を育成する場合につき例を挙げて説明したが、本発明はこれには限定されず、直径１０～１６インチあるいはそれ以上のシリコン単結晶にも適用できる。また、本発明は、シリコン融液に水平磁場、縦磁場、カスプ磁場等を印加するいわゆるＭＣＺ法にも適用できることは言うまでもない。

【００６２】

【発明の効果】以上説明したように、本発明によれば、Ｖ領域、ＯＳＦ領域およびＩ領域のいずれの欠陥領域でもなく、さらにＣｕデポジション処理により検出される酸化膜欠陥も形成されない、高耐圧で優れた電気特性をもつシリコン単結晶ウエーハを安定的に供給することができる。

【図面の簡単な説明】

【図１】本発明の成長速度と結晶欠陥分布の関係を表す説明図である。

【図２】本発明で使用した単結晶引上げ装置の概略図である。

（ａ）装置Ａ、　（ｂ）装置Ｂ。

【図３】（ａ）単結晶成長速度と結晶切断位置の関係を示す関係図である。

（ｂ）各引上げ装置のＯＳＦシュリンク速度を示す説明図である。

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（ｃ）Ｃｕデポジション評価試料の作製方法を示す説明図である。

【図４】本発明で使用した単結晶引上げ装置で育成した単結晶の結晶軸方向のＷＬＴマップである。

（ａ）装置Ａ、　（ｂ）装置Ｂ。

【図５】ＣｕデポジションによりＮｖ領域における欠陥分布を観察した結果図である。

（ａ）Ｃｕデポジション領域、　（ｂ）欠陥のないＮｖ領域。

【図６】Ｎｖ領域内の酸化膜耐圧レベルを測定した結果図である。

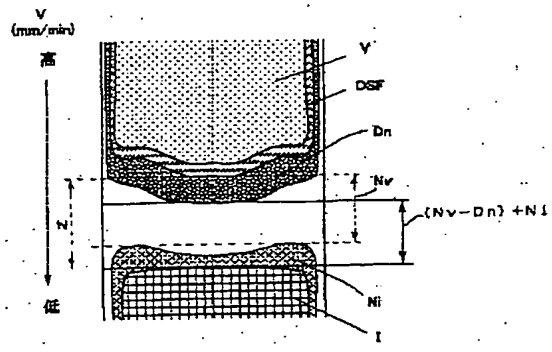
（ａ）Ｃｕデポジションにより欠陥発生領域、　（ｂ）欠陥が発生しなかったＮｖ領域。

【図７】従来の技術による成長速度と結晶の欠陥分布を示す説明図である。

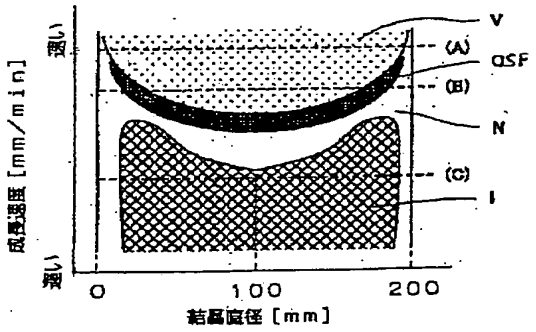
【符号の説明】

１…成長単結晶棒、２…シリコン融液、３…湯面、４…固液界面、６…シードチャック、７…ワイヤ、９…黒鉛筒、１０…外側断熱材、１１…内側断熱筒、１２…黒鉛筒、１３…金属筒、１４…冷却筒、３０…単結晶引上げ装置、３１…引上げ室、３２…ルツボ、３３…ルツボ保持軸、３４…ヒータ、３５…断熱材。Ｖ…Ｖ領域、Ｎ…Ｎ領域、ＯＳＦ…ＯＳＦリング及びＯＳＦ領域、Ｉ…Ｉ領域、Ｎｖ…Ｎｖ領域、Ｎｉ…Ｎｉ領域、Ｄｎ…Ｃｕデポジション欠陥領域。

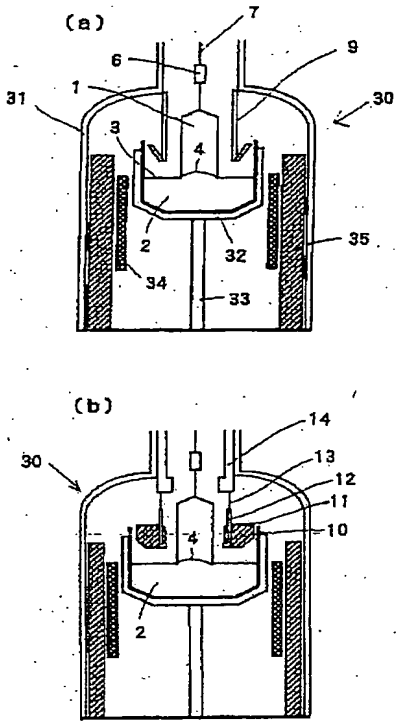
【図１】



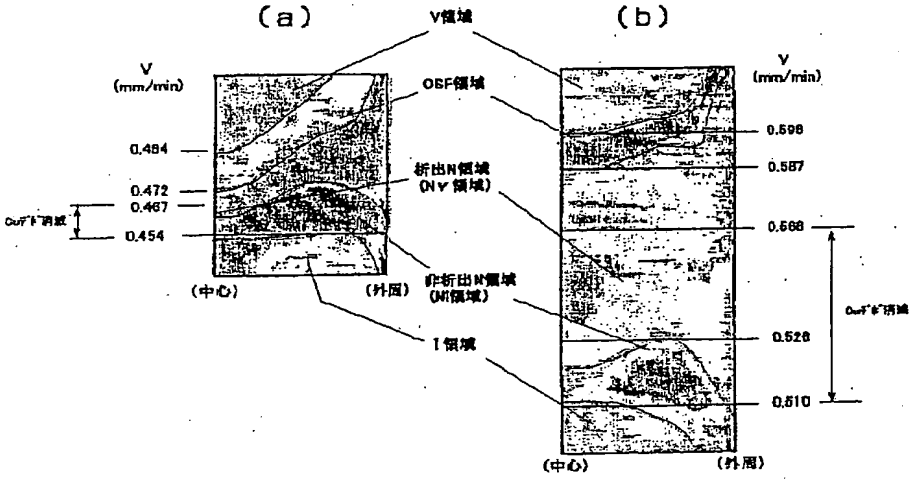
【図７】



【図２】

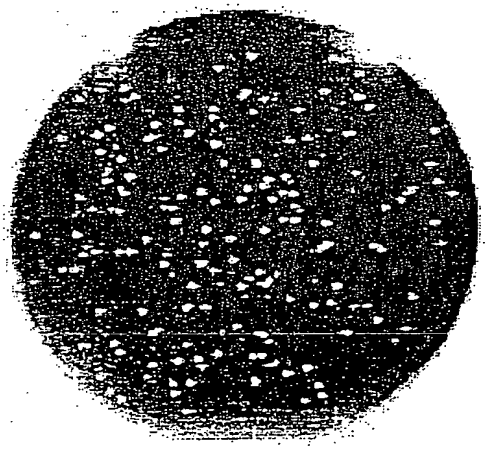

(a)
7
6
9
1
31
30
3
4
2
32
35
34
33
(b)
14
30
13
12
11
10
4
2

【図４】

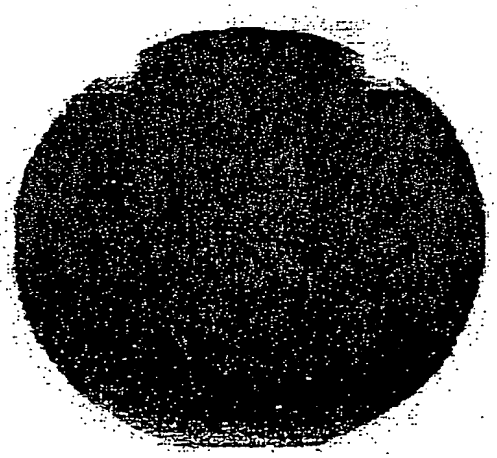

(a)
V領域
(b)
V
(mm/min)
OSF領域
0.484
析出N領域
(Nv領域)
0.472
0.467
0.454
非析出N領域
(Ni領域)
I領域
(中心)
(外周)
V
(mm/min)
0.598
0.587
0.568
0.528
0.510
(中心)
(外周)

【図５】

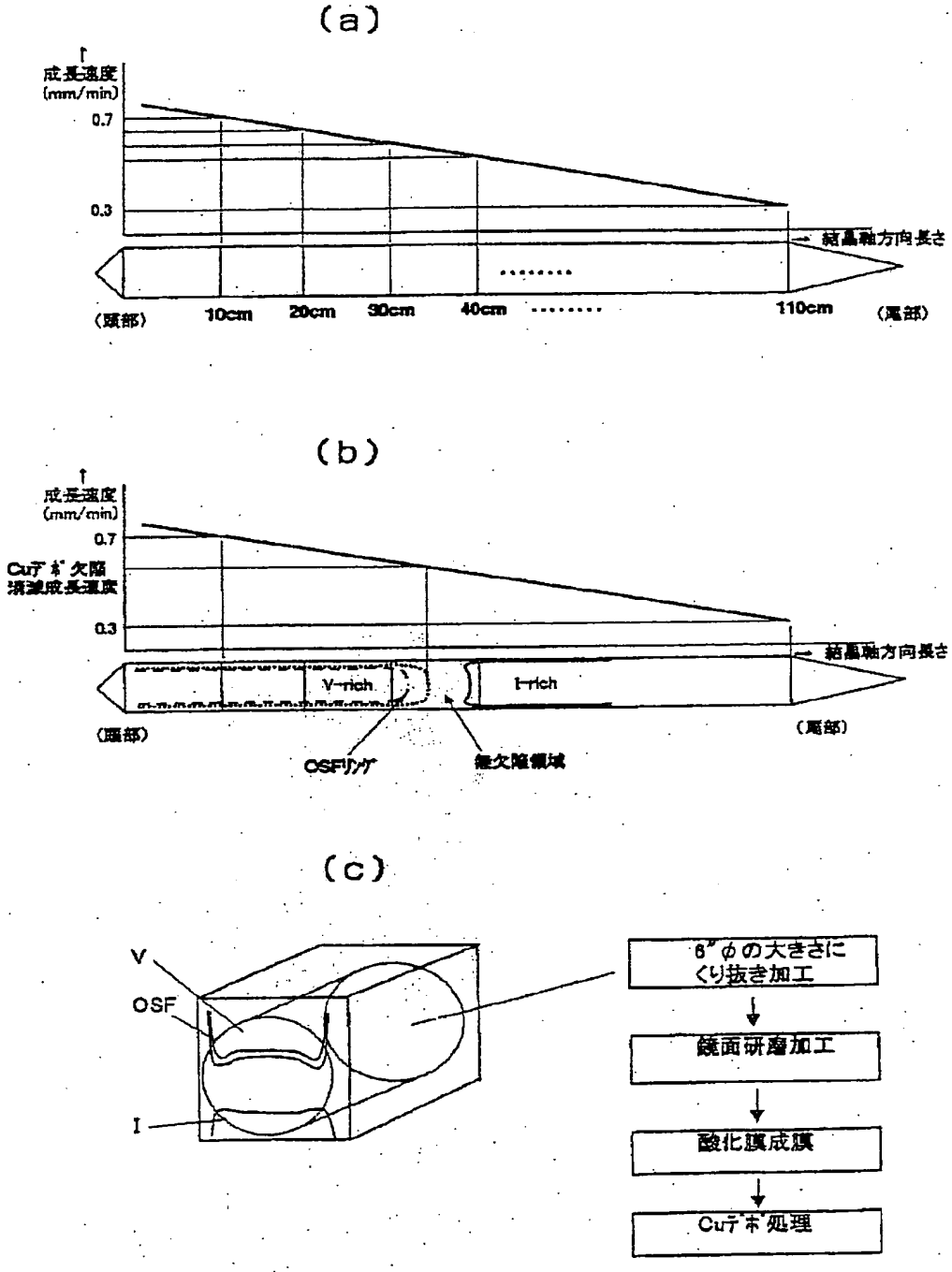
(a)



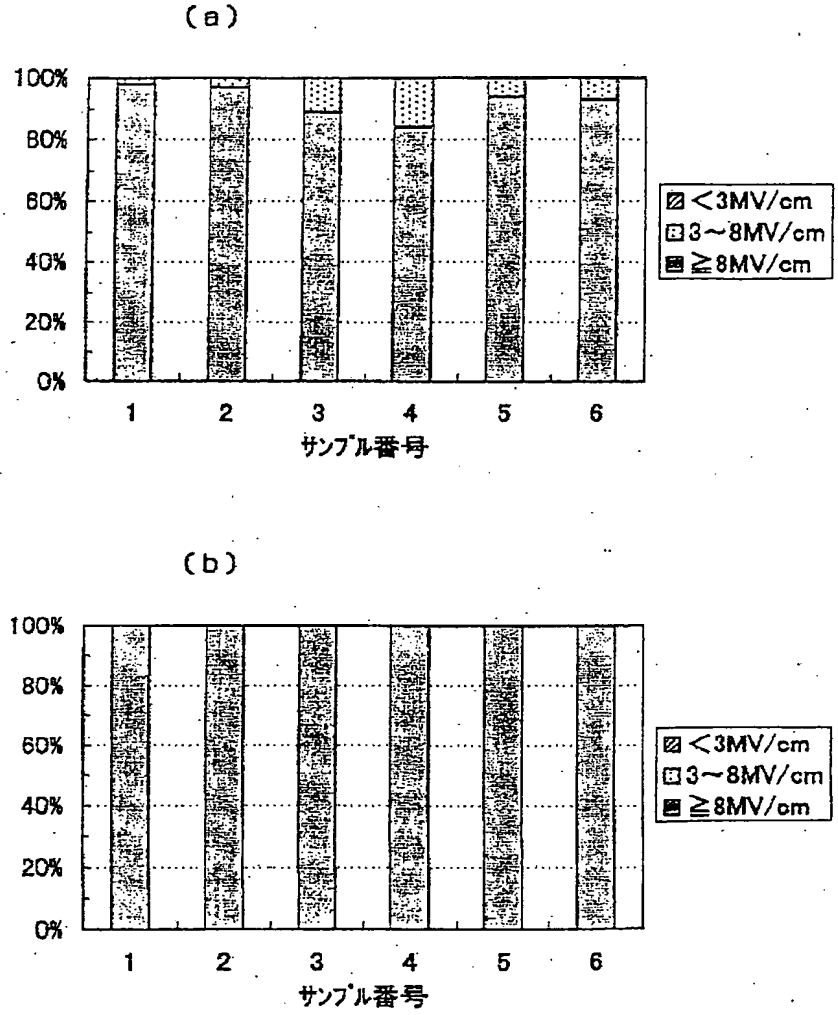
(b)



【図３】


(a)
成長速度
(mm/min)
0.7
0.3
結晶軸方向長さ
(頭部)
10cm
20cm
30cm
40cm
110cm
(尾部)
(b)
成長速度
(mm/min)
0.7
Cuデポ欠陥
消滅成長速度
0.3
結晶軸方向長さ
V-rich
I-rich
(頭部)
(尾部)
OSFリング
無欠陥領域
(c)
V
OSF
I
6"φの大きさに
くり抜き加工
鏡面研磨加工
酸化膜成膜
Cuデポ処理

【図６】



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(54) METHOD OF MANUFACTURING SILICON SINGLE CRYSTAL

(57)Abstract:
PROBLEM TO BE SOLVED: To manufacture a silicon single crystal wafer with the CZ method under stable condition which is capable of improving in electric performance such as oxidation high withstanding voltage surely without belonging to a hole rich V region, an OSF region, and a between lattice silicon rich I region.
SOLUTION: The method of manufacturing silicon single crystal wafer and silicon single crystal are characterized in that in the silicon single crystal water grown by the Czochralski method, in N region out side of OSF ring generated in ring state at the time of heat oxidizing process for all surfaces of the wafer, no defective region is existing which is to be detected by Cu deposition.

LEGAL STATUS

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[Patent number]
[Date of registration]
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[Date of extinction of right]

CLAIMS

[Claim(s)]
[Claim 1] The silicon single crystal wafer characterized by being that in which the defective field which is an N field of the outside of OSF generated in the shape of a ring in the silicon single crystal wafer raised by the Czochrlski method when the whole wafer surface carries out thermal oxidation processing, and is detected by Cu deposition does not exist.
[Claim 2] The silicon single crystal wafer characterized by being N field of the outside of OSF generated in the shape of a ring in the silicon single crystal wafer raised by the Czochrlski method when the whole wafer surface carries out thermal oxidation processing, and being that to which nickel field which the defective field and precipitation of oxygen which are detected by Cu deposition cannot produce easily does not exist in the whole wafer surface.
[Claim 3] The manufacture approach of the silicon single crystal characterized by growing up a crystal in the defect-free field where the defective field which is an N field of the outside of OSF generated in the shape of a ring when thermal oxidation processing is carried out to the silicon single crystal wafer raised when a silicon single crystal was raised with the Czochrlski method, and is detected by Cu deposition does not exist.
[Claim 4] The manufacture approach of the silicon single crystal characterized by to control to the growth rate between the growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when a silicon single crystal is raised with the Czochrlski method and the growth rate of the silicon single crystal under pull-up is dwindled disappears, and the growth rate of the boundary which a grids transition loop formation generates when a growth rate is dwindled further, and to raise a crystal.
[Claim 5] The manufacture approach of the silicon single crystal characterized by growing up a crystal in the field where nickel field which the defective field and precipitation of oxygen which are N field of the outside of OSF generated in the shape of a ring when thermal oxidation processing is carried out to the silicon single crystal wafer raised when a silicon single crystal was raised with the Czochrlski method, and are detected by Cu deposition cannot produce easily does not exist.
[Claim 6] The manufacture approach of the silicon single crystal characterized by to control to the growth rate between the growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when a silicon single crystal is raised with the Czochrlski method and the growth rate of the silicon single crystal under pull-up is dwindled disappears, and the growth rate of the boundary which nickel field which precipitation of oxygen cannot produce easily when a growth rate is dwindled further generates, and to raise a crystal.
[Claim 7] The manufacture approach of the silicon single crystal indicated in any 1 term of claim 3 characterized by making the pull-up rate at the time of said crystal growth into 0.5 or more mm/min thru/or claim 6.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This inventions are not V field which is mentioned later, an OSF field, and which defective field of an I region, either, and relate to the manufacture approach of of the silicon single crystal wafer and silicon single crystal with the electrical property excellent in high pressure-proofing with which the oxide-film defect further detected by copper deposition processing is not formed, either.
[0002]
[Description of the Prior Art] In recent years, the quality demand to the silicon single crystal produced with the Czochrlski method (it is hereafter written as a CZ process) used as the substrate has been increasing with detailed-izing of the component accompanying high integration of a semiconductor circuit. The defect of a single crystal growth reason in which the oxide film proof-pressure property especially called grown-in (Grown-in) defects, such as FPD, LSTD, and COP, and the property of a device are worsened exists, and importance is attached to reduction of the consistency and size.
[0003] In explaining these defects, it explains being known generally about the factor which determines each concentration of the point defect of the hole mold first called the Vacancy (it may outline Vacancy and Following V) incorporated by the silicon single crystal, and the mold silicon point defect between grids called Interstitial-Si (it may outline Interstitial-Si and Following I) incorporated.
[0004] In a silicon single crystal, V fields are Vacancy, i.e., the crevice generated from lack of a silicon atom, and a field with many things like a hole. With an I region It is the thing of a field with many lumps of the rearrangement and the excessive silicon atom which are generated when a silicon atom exists too much. Between V field and an I region The neutral (it may outline Neutral and Following N) field without lack of an atom or an excess (few) will exist. And with [even if said grown-in defects (FPD, LSTD, COP, etc.) occur when V and I are in a condition / ****** / to the last, and it has the bias of some atoms] saturation [below], it has turned out that it does not exist as a defect.
[0005] The concentration of both this point defect is decided from the pull-up rate (growth rate) of the crystal in a CZ process, and relation with the temperature gradient G near [under crystal] the solid-liquid interface. The defect called OSF (an oxidation induction stacking fault, Oxidation Indused Stacking Fault) near [boundary] V field and an I region When it sees in the cross section of the perpendicular direction to a crystal growth shaft, being distributed in the shape of a ring (it being hereafter called an OSF ring) is checked.
[0006] The defect of these crystal growth reason is acquired as a defective distribution map as shown in drawing 7 , when a crystal orientation changes a growth rate from a high speed to a low speed with CZ pull-up machine with which the temperature gradient G near the solid-liquid interface used the large structure in a furnace (hot zone: it may be called HZ) during the usual crystal.
[0007] And a classification of the defect of these crystal growth reason calls V field the field where grown-in defects by which it is considered as the void reason to which hole type point defects gathered when a growth rate is a high speed comparatively, the above before and after 0.6 mm/min and, such as FPD, LSTD, and COP, exist in high density throughout the direction of the diameter of a crystal, for example, and these defects exist (Rhine (A) of drawing 7 R> 7). Moreover, when a growth rate is 0.6 or less mm/min, the field where an OSF ring is generated from the circumference of a crystal, the defect of ratios of length to diameter (Large Dislocation: the cable address of the dislocation loop between grids, LSEPD, LFPD, etc.) considered to be dislocation loop reasons by the outside of this ring exists in a low consistency with the fall of a growth rate, and these defects exist is called the I region (it may be called a ratio-of-length-to-diameter field). Furthermore, if a growth rate is made into a low speed below 0.4 mm/min order, an OSF ring will condense and disappear at the core of a wafer, and the whole surface will serve as an I region (Rhine (c) of drawing 7).
[0008] Moreover, the existence of the field where neither FPD of a hole reason, LSTD, COP nor LSEPD of a dislocation loop reason and LFPD exist called N field to the outside of an OSF ring is discovered in the middle of V field and an I region in recent years. It is reported that this field is the I region side which is not so rich as there is almost no precipitation of oxygen by being in the outside of an OSF ring when oxygen precipitation heat treatment is performed and the contrast of a deposit is checked by X-ray observation etc., and LSEPD and LFPD are formed (Rhine (B) of drawing 7).
[0009] Since these N fields existed aslant to growth shaft orientations by the usual approach when a growth rate is lowered, they existed only in the part in the wafer side. About this N field, it has recited that a parameter called V/G which is the ratio of a pull-up rate (V) and a crystal solid-liquid interface shaft-orientations temperature gradient (G) determines the total concentration of a point defect by the Voronkov theory (V. V.Voronkov;Journal of Crystal Growth, 59 (1982) 625-643). Only a crystal into which a core serves as an I region on the outskirts across N field in V field at a certain pull-up rate since it pulls up in a field, and the rate must be regularity and G has distribution in a field when it thinks from this was obtained.
[0010] Then, distribution of G within a field was improved, and when this N-field where that it is only slanting existed was pulled up lowering for example, the pull-up rate F gradually, the crystal with which N field spread all over width at a certain pull-up rate could be manufactured recently. Moreover, in order to expand the crystal of this whole surface N field in the die-length direction, if a pull-up rate when this N field spreads horizontally is maintained and pulled up, it can attain to some extent. Moreover, when adjusting the pull-up rate in consideration of G changing so that it might be amended and V/G might become fixed to the last as the crystal grew, as it is, the crystal used as a whole surface N field could be expanded also in the growth direction.
[0011] If this N field is classified further, there is a nickel field (field with much silicon between grids) contiguous to Nv field (field with many holes) contiguous to the outside of an OSF ring and an I region, and in Nv field, when thermal oxidation processing is carried out, there are many amounts of precipitation of oxygen, and it turns out that there is almost no precipitation of oxygen in nickel field.

[0012] However, as mentioned above, when thermal oxidation processing was carried out, in spite of having been a whole surface N field and having been the single crystal with which an OSF ring is not generated and FPD and ratio of length to diameter do not exist in the whole surface, it turned out that an oxide-film defect may occur remarkably. And this is the cause of degrading an electrical property like an oxide-film proof-pressure property, it is just inadequate that the conventional whole surface is N field, and the further improvement was desired.
[0013]
[Problem(s) to be Solved by the Invention] then, the thing by which this invention was made in view of such a trouble -- it is -- a hole -- rich V field, an OSF field, and the silicon between grids -- it belongs to neither of a rich I region, and aims at obtaining the silicon single crystal wafer by the CZ process which can raise electrical properties, such as oxide-film pressure-proofing, certainly under the stable manufacture condition.
[0014]
[Means for Solving the Problem] The silicon single crystal wafer which it succeeded in order that this invention might attain said purpose, and is applied to this invention is characterized by being that in which the defective field which is an N field of the outside of OSF generated in the shape of a ring, and is detected by Cu deposition does not exist, when the whole wafer surface carries out thermal oxidation processing in the silicon single crystal wafer raised by the Czochrlski method (claim 1).
[0015] Thus, the silicon single crystal wafer of this invention is a defect-free wafer with which the defective field which is an N field of the outside of OSF generated in the shape of a ring when the whole wafer surface carries out thermal oxidation processing, and is detected by especially Cu deposition does not exist, and turns into a silicon wafer of the high quality which does not degrade electrical properties, such as an oxide-film proof-pressure property, even if it produces a device.
[0016] And the silicon single crystal wafer which is the 2nd mode of this invention is characterized by being N field of the outside of OSF generated in the shape of a ring, when the whole wafer surface carries out thermal oxidation processing, and being that to which nickel field which the defective field and precipitation of oxygen which are detected by Cu deposition cannot produce easily does not exist in the whole wafer surface in the silicon single crystal wafer raised by the Czochrlski method (claim 2).
[0017] Thus, when the whole wafer surface carries out thermal oxidation processing, it is N field of the outside of OSF generated in the shape of a ring, nickel field which the defective field and precipitation of oxygen which are detected by especially Cu deposition cannot produce easily is the defect-free wafer which does not exist in the whole wafer surface, and gettering capacity is also high [a wafer] while it does not degrade electrical properties, such as an oxide-film proof-pressure property, even if the silicon single crystal wafer of this invention produces a device.
[0018] Next, the manufacture approach of the silicon single crystal concerning this invention is characterized by growing up a crystal in the defect-free field where the defective field which is an N field of the outside of OSF generated in the shape of a ring when thermal oxidation processing is carried out to the silicon single crystal wafer raised when a silicon single crystal was raised with the Czochrlski method, and is detected by Cu deposition does not exist (claim 3).
[0019] And the manufacture approach of the silicon single crystal concerning this invention [when raising a silicon single crystal with the Czochrlski method] The growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when the growth rate of the silicon single crystal under pull-up is dwindled disappears, When a growth rate is furthermore dwindled, it is characterized by controlling to the growth rate between the growth rates of the boundary which a grids transition loop formation generates, and raising a crystal (claim 4).
[0020] According to these manufacture approaches, when thermal oxidation processing is carried out to the raised silicon single crystal wafer, it is N field of the outside of OSF generated in the shape of a ring, and the defect-free silicon single crystal wafer with which the defective field which degrades electrical properties, such as oxide-film pressure-proofing detected by especially Cu deposition, does not exist can be manufactured.
[0021] the 2nd mode of the manufacture approach of the silicon single crystal which furthermore apply to this invention be characterize by to grow up a crystal in the field where nickel field which the defective field and the precipitation of oxygen which be N field of the outside of OSF generate in the shape of a ring when thermal oxidation processing be carry out to the silicon single crystal wafer raised when a silicon single crystal be raised with the Czochrlski method , and be detect by Cu deposition cannot produce easily do not exist (claim 5) .
[0022] In addition, the manufacture approach of the silicon single crystal concerning this invention [when raising a silicon single crystal with the Czochrlski method] The growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when the growth rate of the silicon single crystal under pull-up is dwindled disappears, When a growth rate is furthermore dwindled, it is characterized by controlling to the growth rate between the growth rates of the boundary which nickel field which precipitation of oxygen cannot produce easily generates, and raising a crystal (claim 6).
[0023] According to these manufacture approaches, when the whole wafer surface carries out thermal oxidation processing, it is N field of the outside of OSF generated in the shape of a ring, and nickel field which the defective field and precipitation of oxygen which are detected by Cu deposition cannot produce easily can manufacture the defect-free silicon single crystal wafer which does not exist in the whole wafer surface. Therefore, oxide-film pressure-proofing and gettering capacity can obtain a good crystal.
[0024] In these manufacture approaches, it is desirable to make the pull-up rate at the time of crystal growth into 0.5 or more mm/min (claim 7). Thus, the manufacture margin of 0.5 or more mm/min then the defect-free field of this invention, especially the field in which an oxygen sludge layer is formed expands the pull-up rate at the time of crystal growth, and adequate supply becomes possible.
[0025] Hereafter, although explained to a detail per this invention, this invention is not limited to these. In advance of explanation, lessons is taken from each vocabulary, and it explains beforehand.
1) K2 Cr 2O7 after cutting down a wafer from the silicon single crystal rod after growth and etching and removing a surface distortion layer with the mixed liquor of fluoric acid and a nitric acid in FPD (Flow Pattern Defect) A pit and a ripple pattern arise by etching a front face with the mixed liquor of fluoric acid and water (Secco etching). This ripple pattern is called FPD, and the defects of oxide-film pressure-proofing increase in number, so that the FPD consistency within a wafer side is high (refer to JP,4-192345,A).
[0026] 2) When the same Secco etching as FPD is performed, call SEPD (Secco Etch Pit Defect) a thing without FPD, a call, and a flow pattern for the thing accompanied by a flow pattern (flow pattern) with SEPD. When it is thought in this that large SEPD (LSEPD) 10 micrometers or more originates in a rearrangement cluster and a rearrangement cluster exists in a device, a current leaks through this rearrangement and it stops achieving the function as a P-N junction.
[0027] 3) Cut down a wafer from the silicon single crystal rod after growth, and carry out cleavage of the wafer to LSTD (Laser Scattering Tomography Defect) after etching and removing a surface distortion layer with the mixed liquor of fluoric acid and a nitric acid. Incidence of the infrared light can be carried out from this cleavage plane, and the defect scattering light which exists in a wafer can be detected by detecting the light which came out from the wafer front face. About the scatterer observed here, it is a society etc., there is already a report, and it is regarded as the oxygen sludge (Jpn.J.Appl.Phys. Vol.32, P3679, 1993 reference). Moreover, the

result that it is the void (hole) of octahedron is also reported by the latest research.
[0028] 4) the defect which becomes the cause of degrading oxide film pressure-proofing of the core of a wafer, with COP (Crystal Originated Particle) -- it is -- Secco -- by SC-1 washing (washing by the mixed liquor of NH4 OH:H2 O2:H2 O=1:1:10), the defect set to FPD if dirty works as a selection etching reagent, and is set to COP. The diameter of this pit is investigated with light scattering measurement by 1 micrometer or less.
[0029] 5) It is the defect which there are LSEPD, LFPD, etc. in ratio of length to diameter (Large Dislocation: cable address of the dislocation loop between grids), and is considered to be a dislocation loop reason. A large thing 10 micrometers or more is said that LSEPD described above also in SEPD. Moreover, also in FPD which LFPD described above, the magnitude of a tip pit says a large thing 10 micrometers or more, and it is considered the dislocation loop reason also here.
[0030] 6) The Cu deposition method measures the location of the defect of a semiconductor wafer correctly, raises the sensitiveness to the defect of a semiconductor wafer, measures it correctly also to a more detailed defect, and is an appraisal method of the wafer which can be analyzed.
[0031] The concrete evaluation approach of a wafer destroys the insulator layer on the defective part which was made to form the insulator layer of predetermined thickness and was formed near the front face of said wafer on the wafer front face, and deposits electrolysis matter, such as Cu, to a defective part (deposition). That is, the Cu deposition method is an appraisal method using a current flowing to the part to which the oxide film has deteriorated, and Cu ion serving as Cu and depositing in the liquid with which Cu ion is dissolved, if potential is impressed to the oxide film formed in the wafer front face. It is known that defects, such as COP, exist in the part by which an oxide film tends to deteriorate.
[0032] The defective part of the wafer by which Cu deposition was carried out can be analyzed on the bottom of a condensing LGT, or a direct target with the naked eye, can evaluate the distribution and consistency, and can also check microscope observation, a transmission electron microscope (TEM), or a scanning electron microscope (SEM) further.
[0033]
[Embodiment of the Invention] When this invention persons investigated in the detail about the boundary neighborhood of V field and an I region about the silicon single crystal growth by the CZ process, they found out neutral N field where the outside of an OSF ring has few FPD(s), LSTD(s), and COP remarkably, and ratio of length to diameter does not exist in it in the middle of V field and an I region, either. And if this N field is classified further, there is a nickel field (field with much silicon between grids) contiguous to Nv field (field with many holes) contiguous to the outside of an OSF ring and an I region, and in Nv field, when thermal oxidation processing is carried out, there are many amounts of precipitation of oxygen, and it has turned out that there is no precipitation of oxygen in nickel field.
[0034] However, even if it raised the crystal in the above-mentioned N field, there is what has bad oxide-film pressure-proofing, and the cause was not found well. Then, when this invention person etc. investigated in the detail further about N field by the Cu deposition method, he is N field of the outside of an OSF field, and discovered that a part of Nv field which the precipitation of oxygen after precipitation heat treatment tends to generate had the field which the defect detected by Cu deposition processing generates remarkably. And this traced that it was the cause of degrading an electrical property like an oxide-film proof-pressure property.
[0035] Then, if a field without the defective field which is an N field of the outside of this OSF and is detected by Cu deposition can be extended all over a wafer, while said various grown-in defects cannot be found, the wafer which can improve an oxide-film proof-pressure property etc. certainly will be obtained.
[0036] this invention person etc. conducted the following experiments, asked for a growth rate and the relation of defective distribution, raised the single crystal rod based on the result, and evaluated the oxide-film proof-pressure property of a wafer.
(Experiment 1) MCZ shown in the equipment A of drawing 2 (a), and the equipment B of drawing 2 (b) -- law -- among crystal pulling equipment (horizontal magnetic field impression), Equipment A charged 150kg of raw material polycrystalline silicon to the 24 inch quartz crucible, and Equipment B charged 160kg of raw material polycrystalline silicon to 26 inch quartz RUTSUPO, and it pulled up the silicon single crystal of the diameter of 8 inches (diameter of 200mm), and bearing <100> with each equipment. When pulling up a single crystal, it controlled to dwindle a tail from a crystal head in the range of 0.7 mm/min to 0.3 mm/min, applying a growth rate. Moreover, the single crystal was produced so that the oxygen density of a wafer might serve as 22 - 23ppma (ASTM'79 value).
[0037] And as shown in drawing 3 (a) and (b), it applied to the tail from the head of the crystal pulled up, vertical division cutting was carried out in the crystal orientation, and the four wafers sample was produced. Among four sheets, three sheets investigated the distribution situation of each field of V field, an OSF field, and an I region, the distribution situation of FPD and LEP, and the OSF generating situation by OSF heat treatment by WLT (wafer life time) measurement (measuring instrument: SEMILAB WT-85) and SEKOETCHINGU, and checked the growth rate of each field boundary. One in the sample which furthermore carried out vertical division cutting in the crystal orientation ****-omission-processes a wafer configuration with a diameter of 6 inches, as shown in drawing 3 (c), and it is 1. After mirror plane processing finishing, after ** formed the thermal oxidation film in the wafer front face, it performed Cu deposition processing and checked the distribution situation of an oxide film defect.
[0038] The evaluation procedure of the wafer in this experiment and detail of an evaluation result are given below.
(1) Vertical division cutting of the single crystal rod pulled up was carried out after block cutting in vertical crystal orientation at the die length for 10cm of every crystal orientation, and four samples of about 2mm thickness were produced.
(2) In the wafer heat treating furnace, 800 degrees C and 4-hour (under nitrogen-gas-atmosphere mind) heat treatment were performed after heat treatment to the bottom of nitrogen-gas-atmosphere mind, it cooled after that after 1000 degrees C and 16-hour (under dry oxygen ambient atmosphere) heat treatment, and the 1st in the above-mentioned sample created the map of wafer life time (WLT) by SEMILAB-85 for 620 degrees C and 2 hours (refer to drawing 4 (a) and (b)). Moreover, the 2nd sheet gave SEKOETCHINGU after mirror etching, and observed distribution of FPD and LEP. And the 3rd sheet, it removed the oxide film, and checked the distribution situation of OSF. [after OSF heat treatment] Each field of V field, an OSF field, and an I region was pinpointed from these results, and the growth rate of each boundary was investigated.
[0039] The growth rate (refer to drawing 4 (a)) of each boundary of the single crystal pulled up with Equipment A (drawing 2 (a)) was as follows.
V field / OSF field boundary: 0.484 mm/min OSF disappearance boundary: 0.472 mm/min Cu deposition defective disappearance boundary: 0.467 mm/min Non-depositing N(nickel) field / I region boundary: 0.454 mm/min, [0040] The growth rate (refer to drawing 4 (b)) of each boundary of the single crystal pulled up with Equipment B (drawing 2 (b)) is as follows.
V field / OSF field boundary: 0.596 mm/min OSF disappearance boundary: 0.587 mm/min Cu deposition defective disappearance boundary: 0.566 mm/min A deposit N(Nv) field / nickel field boundary: 0.526 mm/min nickel field / I region boundary : 0.510 mm/min, [0041] (3) the sample which carried out vertical division cutting in the crystal orientation of the single crystal rod of the

above (1) -- inner -- **** omission processing (refer to drawing 3 (c)) of remaining one sheet was carried out to the wafer configuration with a diameter of 6 inches, Cu deposition processing after thermal oxidation film formation was performed to the wafer front face after mirror plane processing finishing, and the distribution situation of an oxide film defect was checked. The evaluation conditions are as follows.
1) Oxide film : 25nm 2 electrolysis reinforcement: For [6 MV/cm and 3 electrical-potential-difference impression time amount:] 5 minutes.
[0042] A Fig. is shown as a result of Cu deposition's estimating Nv field to drawing 5 . Drawing 5 (a) shows defective distribution of Nv field without the defect according [(b)] defective distribution of the defective field generated by Cu deposition to Cu deposition. Drawing 6 (a) is as a result of [of Nv field which the defect generated in Cu deposition] evaluation, and (b) is as a result of [of Nv field which a defect did not generate by Cu deposition] evaluation.
[0043] It turns out that the defective field detected by Cu deposition which an oxide film defect tends to produce all over Nv field which precipitation of oxygen tends to produce from the above result among N fields which exist in an OSF outside exists. In this field, in spite of being Nv field, oxide-film pressure-proofing is not necessarily good. It turns out that a result which can be satisfied also with the same Nv field of oxide-film pressure-proofing in Nv field without the defective field detected by this Cu deposition on the other hand is brought.
[0044] (Experiment 2) Next, based on the above-mentioned result, using Equipment B (drawing 2 (b)), it was N field of an OSF outside, it was processed into the wafer of mirror plane finishing from the crystal which controlled the growth rate and pulled up so that the field which does not include the field and nickel field which precipitation of oxygen cannot produce further easily which is not Cu deposition defective field (Dn field), either might be aimed at, and the oxide film proof pressure property was evaluated. In addition, the C-mode Measuring condition is as follows.
1) Oxide film : 25nm Two measuring electrode: The Lynn dope polish recon and 3 electrode-surface product:8mm2 4 judging current: 1mA/cm2.
Consequently, oxide film proof-pressure level was 100% of rate of an excellent article.
[0045] this invention person etc. repeats examination wholeheartedly, after being based on the knowledge acquired in the above experiment, and he hits on an idea to this invention. The manufacture approach of the 1st silicon single crystal of this invention is characterized by growing up a crystal in the defect-free field where the defective field which is an N field of the outside of OSF generated in the shape of a ring when thermal oxidation processing is carried out to the raised silicon single crystal wafer, and is detected by Cu deposition does not exist.
[0046] It will control to the growth rate between the growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when this approach was explained based on drawing 1 and the growth rate of the silicon single crystal under pull-up is dwindled disappears, and the growth rate of the boundary which a grids transition loop formation generates when a growth rate is dwindled further, and a crystal will be raised.
[0047] The wafer cut down from the single crystal rod raised by the approach described above turns into a defect-free silicon single crystal wafer with which the defective field which is an N field of the outside of OSF generated in the shape of a ring when the whole wafer surface carries out thermal oxidation processing, and is detected by Cu deposition does not exist at all.
[0048] Next, when the 2nd manufacture approach carries out thermal oxidation processing to the raised silicon single crystal wafer, it is N field of the outside of OSF generated in the shape of a ring, and it is characterized by growing up a crystal in the field where nickel field which the defective field and precipitation of oxygen which are detected by Cu deposition cannot produce easily does not exist.
[0049] It will control to the growth rate between the growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when this approach was explained based on drawing 1 and the growth rate of the silicon single crystal under pull-up is dwindled disappears, and the growth rate of the boundary which nickel field which precipitation of oxygen cannot produce easily when a growth rate is dwindled further generates, and a crystal will be raised.
[0050] The wafer produced from the single crystal rod raised by this manufacture approach is N field of the outside of OSF generated in the shape of a ring, when the whole wafer surface carries out thermal oxidation processing, and nickel field which the defective field and precipitation of oxygen which are detected by Cu deposition cannot produce easily can use it as the defect-free silicon single crystal wafer which does not exist in the whole wafer surface.
[0051] Since this wafer is Nv field altogether, when it is heat-treated under nitrogen and a dry oxygen ambient atmosphere all over a defect-free field excluding nickel field which precipitation of oxygen cannot produce easily, an oxygen sludge layer is formed into bulk. Therefore, the silicon single crystal wafer produced from this field has the gettering capacity which oxide-film pressure-proofing etc. is not only good, but was excellent.
[0052] When producing this invention article furthermore, when using CZ pull-up equipment of quenching structure which can be raised with the growth rate of 0.5 or more mm/min, the defect-free field of this invention, especially the field (Nv-Dn) in which an oxygen sludge layer is formed were able to expand more the silicon single crystal used as a raw material, and manufacture top stability was able to be maintained.
[0053] And the shaft-orientations temperature gradient Gc of the crystal solid-liquid interface in the crystal center section is small. Although it was not able to mass-produce easily since the growth rate margin of this invention article was less than 0.02 mm/min when it was CZ process pull-up equipment by which the growth rate of 0.5 mm/min is not exceeded at the time of defect-free field manufacture of this invention Gc was large, and in case it was defect-free field manufacture of this invention, when it was CZ process pull-up equipment which can attain the growth rate of 0.5 or more mm/min, the growth rate margin of this invention article is 0.02 or more mm/min, and was able to attain the maximum about 0.05 mm/min. When this invention article was especially manufactured with the growth rate of 0.5 or more mm/min as mentioned above, it turned out that the growth rate margin of the field where an oxygen sludge layer is formed into BARUGU after heat treatment in nitrogen and a dry oxygen ambient atmosphere can be expanded easily.
[0054] Drawing 2 (a) and (b) explain the example of a configuration of the crystal pulling equipment by the CZ process finally used by this invention. As shown in drawing 2 (a), this crystal pulling equipment 30 The pull-up room 31, the crucible 32 prepared all over the pull-up room 31, and the heater 34 arranged around a crucible 32, It has the reel style (not shown) which rotates or rolls round the crucible maintenance shaft 33 made to rotate a crucible 32 and its rolling mechanism (not shown), the seed chuck 6 holding the seed crystal of silicon, the wire 7 that pulls up a seed chuck 6, and a wire 7, and is constituted. A quartz crucible is prepared in the side in which a crucible 32 holds the silicon melt (molten bath) 2 of the inside, and the graphite crucible is prepared in the outside. Moreover, the heat insulator 35 is arranged around [outside] the heater 34.
[0055] Moreover, in order to set up the manufacture conditions in connection with the manufacture approach of this invention, the annular graphite cylinder (thermal insulation plate) 9 is formed. Moreover, what was shown in drawing 2 (b) has formed the annular outside heat insulator 10 in the periphery of the solid-liquid interface 4 of a crystal. This outside heat insulator 10 prepares spacing of

2-20cm between that lower limit and surface of hot water 3 of silicon melt 2, and is installed in it. Furthermore, coolant gas may be sprayed or the tubed cooling system which interrupts radiant heat and cools a single crystal may be formed. Independently, by installing the magnet which is not illustrated in the horizontal outside of the pull-up room 31, and impressing magnetic fields, such as a horizontal direction or a perpendicular direction, to silicon melt 2, the convection current of melt is controlled and, recently, the so-called MCZ method for measuring the stable growth of a single crystal is used in many cases.

[0056] Next, the single-crystal-growth approach by above crystal pulling equipment 30 is explained. First, within a crucible 32, the high grade polycrystal raw material of silicon is heated more than the melting point (about 1420-degreeC), and is dissolved. Next, the tip of seed crystal is made contacted or immersed in the surface abbreviation core of melt 2 by beginning to roll a wire 7. Then, while rotating the crucible maintenance shaft 33 in the proper direction, single crystal growth is started by rolling round rotating a wire 7 and pulling up seed crystal. Henceforth, the single crystal rod 1 of an approximate circle column configuration can be obtained by adjusting a pull-up rate and temperature appropriately.

[0057] In this case, in this invention, especially in order to attain the purpose of this invention, as shown in drawing 2 (a) or drawing 2 R> 2 (b), in the periphery space of the liquefied part in the single crystal rod 1 on the surface of hot water of the pull-up room 31, it is important to have formed the annular graphite cylinder (thermal insulation plate) 9 and the outside heat insulator 10 so that the temperature region from the melting point of the crystal near the surface of hot water to 1400 degrees C could be controlled.

[0058] Namely, what is necessary is to form the outside heat insulator 10 in the pull-up room 31, and just to set spacing on this lower limit and the front face of melt as 2-20cm, in order to control whenever [this furnace temperature], for example, as shown in drawing 2 (b). If it carries out like this, whenever [furnace temperature] is also controllable so that the difference of the temperature gradient Gc of a crystal center part [**/cm] and the temperature gradient germanium of a crystal circumference part becomes small, for example, the direction of the temperature gradient of the crystal circumference becomes lower than a crystal center. This outside heat insulator 10 is in the outside of the graphite cylinder 12, and has formed the heat insulation cylinder 11 also inside the graphite cylinder 12. Moreover, the graphite cylinder 12 top is connected with the metal cylinder 13, and a cooling dome 14 is on it, and it is pouring and carrying out forced cooling of the cooling medium.

[0059] When the silicon single crystal wafer which slices the silicon single crystal manufactured by the manufacture approach of the silicon single crystal described above, and is obtained carries out thermal oxidation processing to a wafer, it is a defect-free wafer with which the defective field which is an N field of the outside of OSF generated in the shape of a ring, and is detected by Cu deposition does not exist. Or when the whole wafer surface carries out thermal oxidation processing, it is N field of the outside of OSF generated in the shape of a ring, and nickel field which the defective field and precipitation of oxygen which are detected by Cu deposition cannot produce easily is the defect-free wafer which does not exist in the whole wafer surface.

[0060] In addition, this invention is not limited to the above-mentioned operation gestalt. The above-mentioned operation gestalt is instantiation, and no matter it may be what thing which has the same configuration substantially with the technical thought indicated by the claim of this invention, and does the same operation effectiveness so, it is included by the technical range of this invention.

[0061] For example, in the above-mentioned operation gestalt, although the example was given and explained per when a silicon single crystal with a diameter of 8 inches was raised, this invention is not limited to this but can be applied also to the diameter of 10-16 inches, or the silicon single crystal beyond it. Moreover, it cannot be overemphasized that this invention is applicable also to the so-called MCZ method for impressing a level magnetic field and length magnetic field, a cusp field, etc. to silicon melt.

[0062]

[Effect of the Invention] As explained above, according to this invention, it is not V field, an OSF field, and which defective field of an I region, either, and the silicon single crystal wafer with the electrical property excellent in high pressure-proofing with which the oxide-film defect further detected by Cu deposition processing is not formed, either can be supplied stably.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is an explanatory view showing the growth rate of this invention, and the relation of crystal defect distribution.
[Drawing 2] It is the schematic diagram of the crystal pulling equipment used by this invention.
(a) Equipment A (b) equipment B.
[Drawing 3] (a) It is the related Fig. showing the relation between a single crystal growth rate and a crystal cutting location.
(b) It is the explanatory view showing the OSF shrink rate of each pull-up equipment.
(c) It is the explanatory view showing the production approach of Cu deposition evaluation sample.
[Drawing 4] It is the WLT map of the crystal orientation of the single crystal raised with the crystal pulling equipment used by this invention.
(a) Equipment A (b) equipment B.
[Drawing 5] It is a Fig. as a result of observing the defective distribution in Nv field by Cu deposition.
(a) Cu deposition field Nv field without the (b) defect.
[Drawing 6] It is a Fig. as a result of measuring the oxide film proof-pressure level in Nv field.
(a) It is a defective generating field by Cu deposition. Nv field which the (b) defect did not generate.
[Drawing 7] It is the explanatory view showing the defective distribution of a growth rate and a crystal by the Prior art.
[Description of Notations]
1 -- a growth single crystal rod, 2 -- silicon melt, 3 -- surface of hot water, and 4 -- a solid-liquid interface, 6 -- seed chuck, 7 -- wire, and 9 -- a graphite cylinder, 10 -- outside heat insulator, 11 -- inside heat insulation cylinder, and 12 -- a graphite cylinder, 13 -- metal cylinders, 14 -- cooling dome, and 30 -- crystal pulling equipment, 31 -- pull-up room, 32 -- crucible, and 33 -- a crucible maintenance shaft, 34 -- heater, and 35 -- heat insulator. A V--V field, a N--N field, an OSF--OSF ring and an OSF field, I -- An I region, a Nv--Nv field, a nickel--nickel field, Dn--Cu deposition defective field.

[Translation done.]

* NOTICES *

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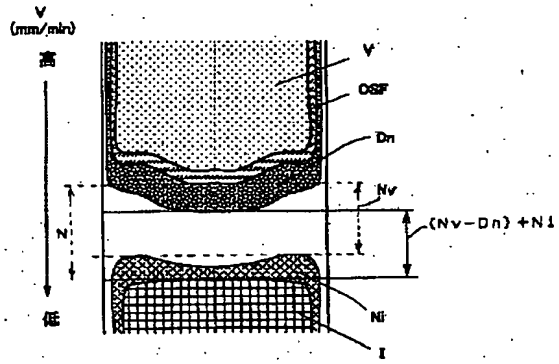
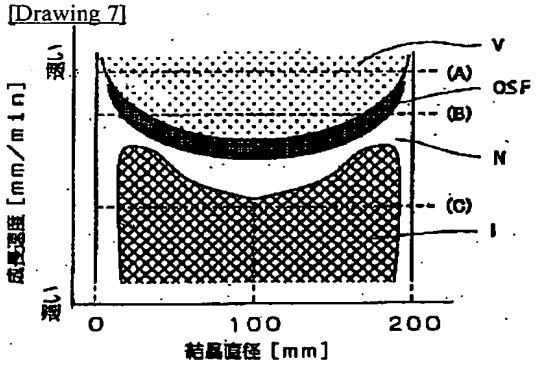
DRAWINGS

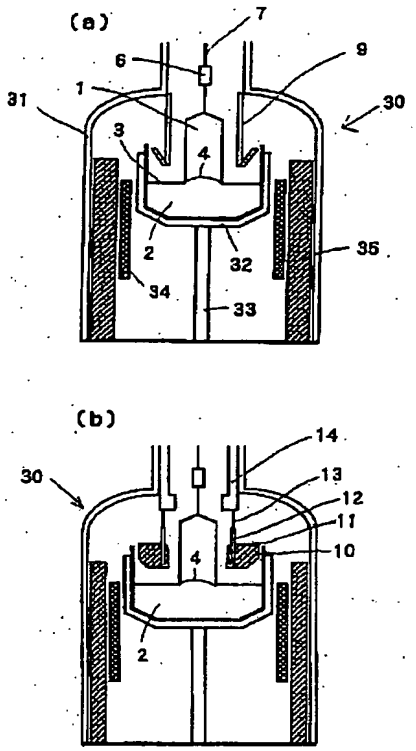
[Drawing 1]



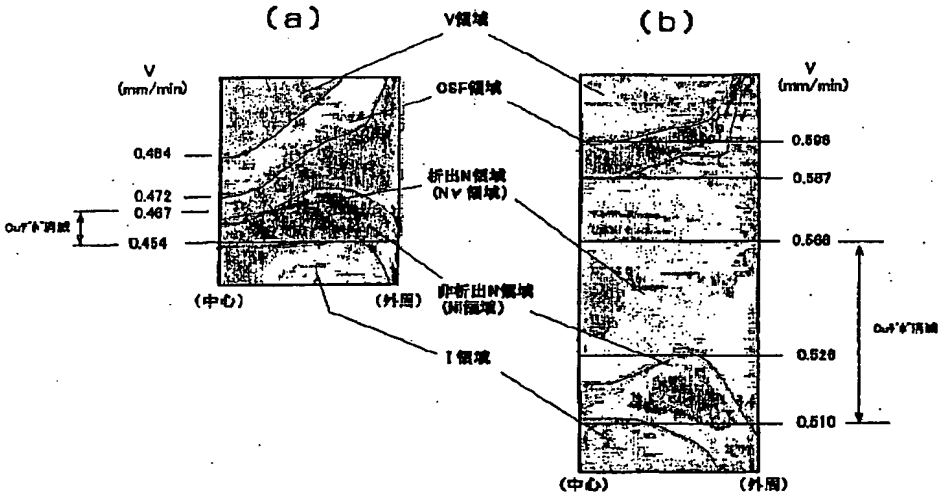
[Drawing 7]



[Drawing 2]

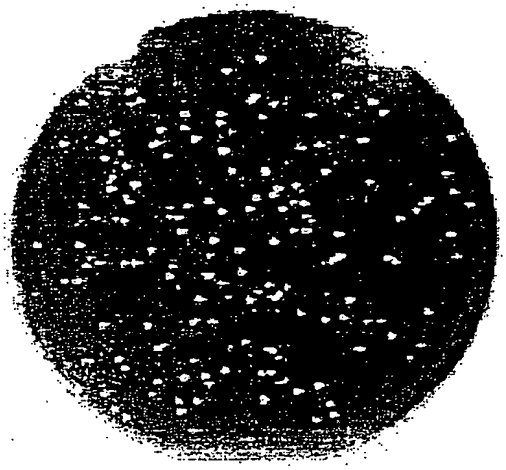


[Drawing 4]

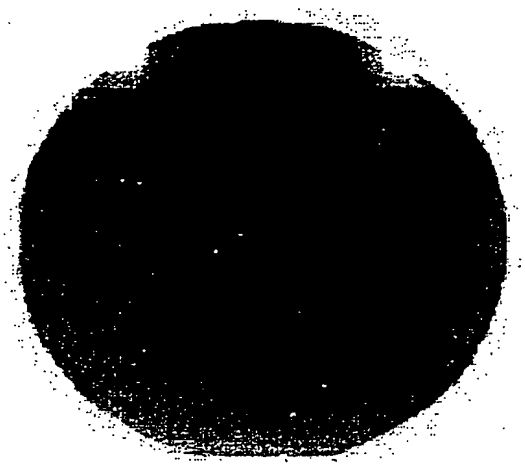


[Drawing 5]

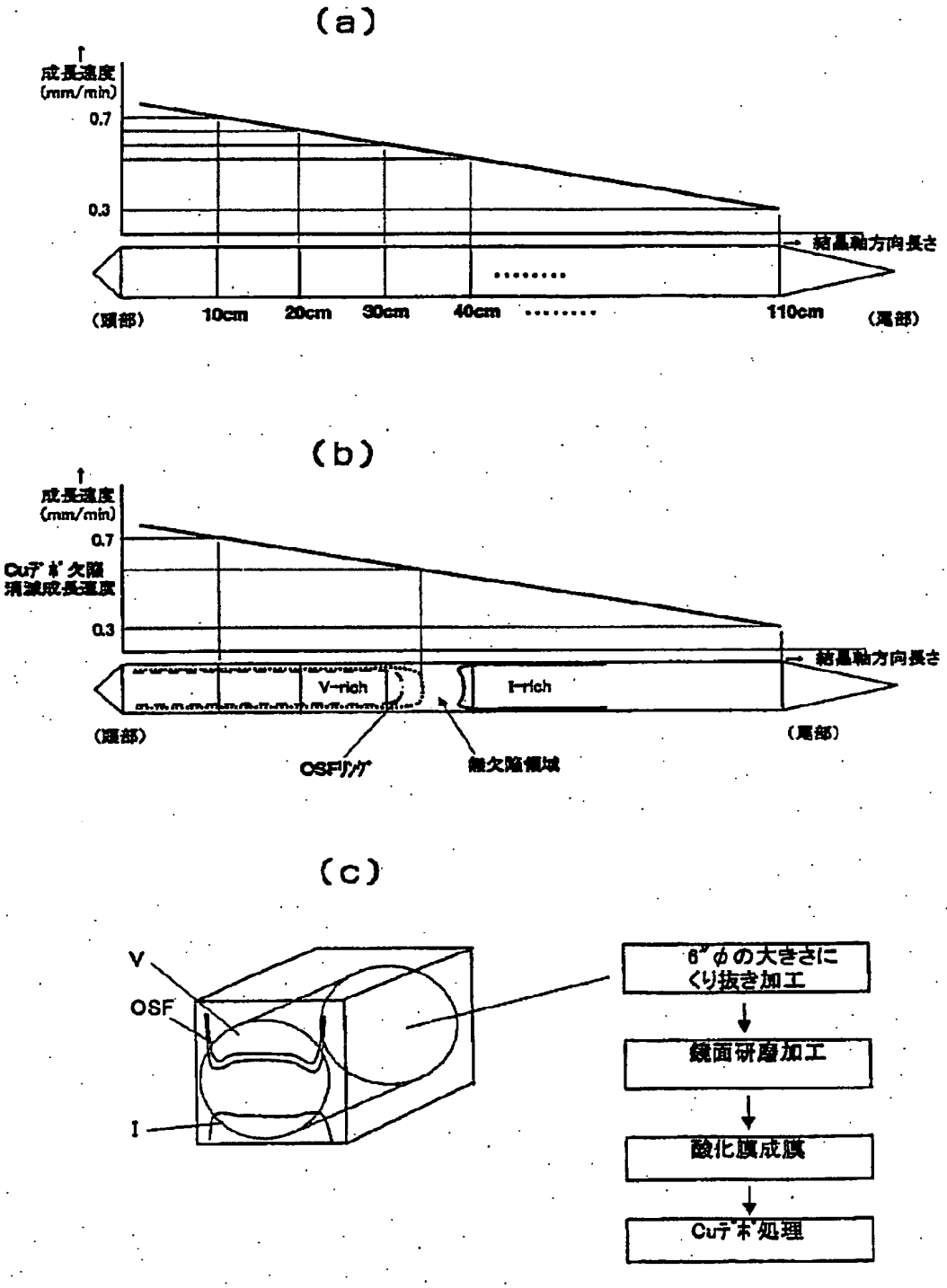
(a)



(b)

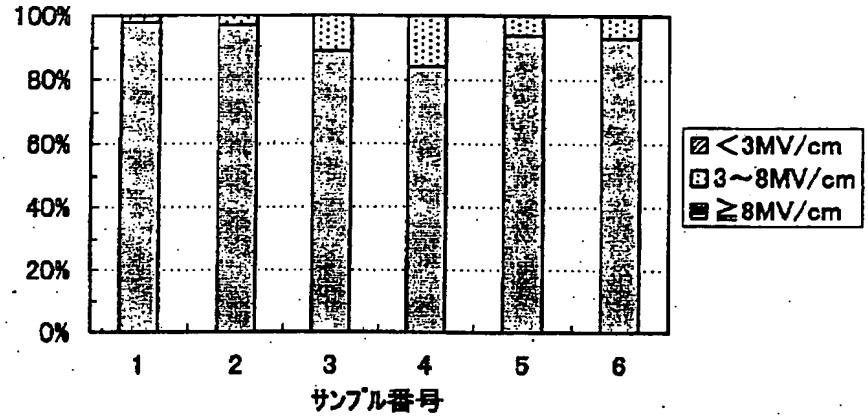


[Drawing 3]

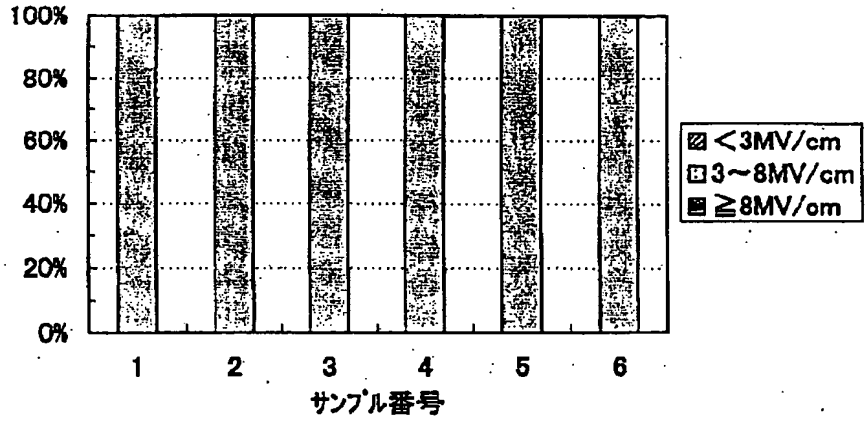

(a)
成長速度
(mm/min)
0.7
0.3
結晶軸方向長さ
(頭部)
10cm
20cm
30cm
40cm
110cm
(尾部)
(b)
成長速度
(mm/min)
0.7
Cuデポ欠陥
消滅成長速度
0.3
結晶軸方向長さ
V-rich
I-rich
(頭部)
(尾部)
OSFリング
(c)
V
OSF
I
6"φの大きさに
くり抜き加工
鏡面研磨加工
酸化膜成膜
Cuデポ処理

[Drawing 6]

(a)



(b)



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CORRECTION OR AMENDMENT

[Kind of official gazette] Printing of amendment by the convention of 2 of Article 17 of Patent Law
[Section partition] The 1st partition of the 3rd section
[Publication date] July 30, Heisei 15 (2003. 7.30)

[Publication No.] JP,2002-201093,A (P2002-201093A)
[Date of Publication] July 16, Heisei 14 (2002. 7.16)
[Annual volume number] Open patent official report 14-2011
[Application number] Application for patent 2000-403127 (P2000-403127)
[The 7th edition of International Patent Classification]

C30B 29/06 502
H01L 21/208
21/66

[FI]

C30B 29/06 502 J
H01L 21/208 P
21/66 N

[Procedure revision]
[Filing Date] April 25, Heisei 15 (2003. 4.25)
[Procedure amendment 1]
[Document to be Amended] Specification
[Item(s) to be Amended] Claim 4
[Method of Amendment] Modification
[Proposed Amendment]
[Claim 4] The manufacture approach of the silicon single crystal characterized by to control to the growth rate between the growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when a silicon single crystal is raised with the Czochrlski method and the growth rate of the silicon single crystal under pull-up is dwindled disappears, and the growth rate of the boundary which the dislocation loop between grids generates when a growth rate is dwindled further, and to raise a crystal.
[Procedure amendment 2]
[Document to be Amended] Specification
[Item(s) to be Amended] 0010
[Method of Amendment] Modification
[Proposed Amendment]
[0010] Then, distribution of G within a field was improved, and when this N-field where that it is only slanting existed was pulled up lowering for example, the pull-up rate V gradually, the crystal with which N field spread all over width at a certain pull-up rate could be manufactured recently. Moreover, in order to expand the crystal of this whole surface N field in the die-length direction, if a pull-up rate when this N field spreads horizontally is maintained and pulled up, it can attain to some extent. Moreover, when adjusting the pull-up rate in consideration of G changing so that it might be amended and V/G might become fixed to the last as the crystal grew, as it is, the crystal used as a whole surface N field could be expanded also in the growth direction.
[Procedure amendment 3]
[Document to be Amended] Specification
[Item(s) to be Amended] 0019
[Method of Amendment] Modification
[Proposed Amendment]
[0019] And the manufacture approach of the silicon single crystal concerning this invention, It is characterized by controlling to the growth rate between the growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when a silicon single crystal is raised with the Czochrlski method and the growth rate of the silicon single crystal under pull-up is dwindled disappears, and the growth rate of the boundary which the dislocation loop between grids generates when a growth rate is dwindled further, and raising a crystal (claim 4).
[Procedure amendment 4]
[Document to be Amended] Specification
[Item(s) to be Amended] 0041
[Method of Amendment] Modification
[Proposed Amendment]
[0041] (3) the sample which carried out vertical division cutting in the crystal orientation of the single crystal rod of the above (1) –

inner -- **** omission processing (refer to drawing 3 (c)) of remaining one sheet was carried out to the wafer configuration with a diameter of 6 inches, Cu deposition processing after thermal oxidation film formation was performed to the wafer front face after mirror plane processing finishing, and the distribution situation of an oxide film defect was checked.
The evaluation conditions are as follows.
1) Oxide film : 25nm 2 field strength: 6 MV/cm,
3) Electrical-potential-difference impression time amount : for 5 minutes.
[Procedure amendment 5]
[Document to be Amended] Specification
[Item(s) to be Amended] 0046
[Method of Amendment] Modification
[Proposed Amendment]
[0046] It will control to the growth rate between the growth rate of the boundary where the defective field detected by Cu deposition which remains after OSF ring disappearance when this approach was explained based on drawing 1 and the growth rate of the silicon single crystal under pull-up is dwindled disappears, and the growth rate of the boundary which the dislocation loop between grids generates when a growth rate is dwindled further, and a crystal will be raised.

[Translation done.]

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